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SIGNAL PROCESSING/HGCDTE INTERCONNECT STUDY FOR MOSAIC SENSOR F--ETC(U)
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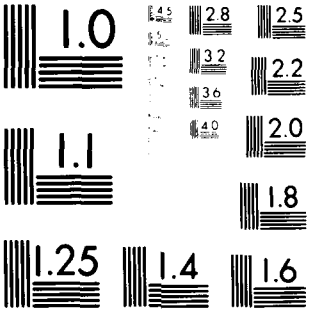

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SECURITY CLASSIFICATION OF THIS PAGE (When Data Entered)

18 19 REPORT DOCUMENTATION PAGE

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1. REPORT NUMBER: AFOSR-TR- 81-0433

2. GOVT ACCESSION NO.: AD-A098821

3. RECIPIENT'S CATALOG NUMBER:

4. TITLE (and Subtitle): 6 SIGNAL PROCESSING/HgCdTe INTERCONNECT STUDY FOR MOSAIC SENSOR FOCAL PLANES.

5. TYPE OF REPORT & PERIOD COVERED: (FINAL) 20 OCTOBER 1980 THRU 20 JANUARY 1981

6. PERFORMING ORG. REPORT NUMBER:

7. AUTHOR(s): 10 KIRK D. KEER, DONALD J. CARLSON, ALAN LEE, A. DEAN MARKUM, R. SPENCER SPRIGGS

8. CONTRACT OR GRANT NUMBER(s): 15 F49620-81-C-0019

9. PERFORMING ORGANIZATION NAME AND ADDRESS:
GRUMMAN AEROSPACE CORPORATION
2852 KELVIN AVENUE
IRVINE, CALIFORNIA 92714

10. PROGRAM ELEMENT, PROJECT, TASK AREA & WORK UNIT NUMBERS: 61102F

11. CONTROLLING OFFICE NAME AND ADDRESS:
DIRECTOR, ELECTRONIC & MATERIAL SCIENCES
AIR FORCE OFFICE OF SCIENTIFIC RESEARCH, ATTN: NE
BLDG 410, BOLLING AFB, WASHINGTON, D.C. 20332

12. REPORT DATE: 11 13 APRIL 1981

13. NUMBER OF PAGES: 31

14. MONITORING AGENCY NAME & ADDRESS (if different from Controlling Office): 12 38

15. SECURITY CLASS. (of this report): UNCLASSIFIED

15a. DECLASSIFICATION/DOWNGRADING SCHEDULE:

16. DISTRIBUTION STATEMENT (of this Report):
APPROVED FOR PUBLIC RELEASE; DISTRIBUTION UNLIMITED

IC-L-181-05

17. DISTRIBUTION STATEMENT (of the abstract entered in Block 20, if different from Report):

18. SUPPLEMENTARY NOTES:

19. KEY WORDS (Continue on reverse side if necessary and identify by block number):

20. ABSTRACT (Continue on reverse side if necessary and identify by block number):

SEE NEXT PAGE

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ABSTRACT

During the conduct of this study, Grumman has addressed the following in terms of conceptual design:

- o Z-Technology Module Design
  - Basic Circuit Design
  - Stacking Technique
  - Thermal Control
- o Signal Processing Chip Design and
  - Basic Circuit Design
  - Physical Thinning
- o Detector Array Design (PV HgCdTe),
  - Determination of Carrier Material
  - Size Optimization

Analyses performed in conjunction with the above included:

- o Thermal Loads
- o Electrical Performance Analysis of CCD and
  - Gain
  - Noise
  - Dynamic Range
- o Array to Module Bonding
  - Indium Metallization
  - Etching/Delineation Methods
  - Alignment Technique
  - Material Properties & Process Analysis

The conclusion of our study is that the combination of HgCdTe and Z-technology modules can provide significant improvement in inter-module fill factor, larger dynamic range and improved clutter rejection plus greater flexibility in relative amount of on-focal plane signal processing when compared to planar arrays. We believe this effort to have been an important step in the progress of HgCdTe technology which will ultimately provide the next generation surveillance system.

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REPORT NO. IC-L-481-053

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FINAL REPORT

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PREPARED FOR

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AIR FORCE OFFICE OF SCIENTIFIC RESEARCH
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BUILDING 410
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	1	N/A	F49620-81-C-0019

REPORT

NO. IC-L-481-053 DATE: April 13, 1981

SIGNAL PROCESSING/HgCdTe INTERCONNECT STUDY FOR MOSAIC FOCAL PLANES

CODE 26512

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REVISIONS

DATE	REV. BY	REVISIONS & ADDED PAGES	REMARKS

GAC 324A REV. 3
10-70

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TABLE OF CONTENTS

SECTION	TITLE	PAGE
	DD Form 1473/Abstract	i
	Table of Illustrations	iii
1.0	Introduction	1
2.0	Research Objective	7
3.0	Signal Processing Concept	8
4.0	Detector Array Attachment Concept	20
5.0	Risk Areas	30
6.0	Summary	30

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TABLE OF ILLUSTRATIONS

FIGURE	TITLE	PAGE
1	Mosaic Focal Plane/Signal Processing Configurations	3
2	Z-Technology Approach	9
3	Hybrid/Planar Approach	9
4	Peak Detection/Signal Processing Multiplexer	10
5	General Multiplexing Scheme	12
6	Transimpedance Amplifier	14
7	Peak Detector	15
8	CMOS Comparator	16
9	Latch and Timer Structure	17
10	Latch and Timer Timing	18
11	Microprocessor Controller Function Flow Chart	19
12	Z-Technology Focal Plane Module	21
13	Relationship of Detector Array to Module Bonding Pads	22
14	Cutaway of Bump Bonded Array	24
15	Exploded View of Bump Bonded Array	24
16	Cold Weld Bump Bonding (Like Materials)	25
17	Cold Weld Bump Bonding (Different Materials)	25
18	Cutaway of NERC Approach to Array/Module Interface	26
19	Alternate Approach for Small Quantity	27

1.0 Introduction

Infrared focal plane technology has made impressive progress over the last few years. Demand to continually increase detector performance will continue, but future increases are very difficult as we are approaching the theoretical performance limits. The number of detectors that can be economically and reliably incorporated on the focal plane has limited the performance. Space applications of the future will require higher sensitivity and extremely high resoltuion and this can only be met by increasing the number of detectors and/or increasing the integration time. The high density mosaic focal plane is the ultimate device to meet these needs. It can provide the required sensitivity because of the large number of elements. The staring capability will permit easier signal integration and greater signal-to-noise ratio. The smaller sized elements will increase resolution and the fast electronic scanning will replace mechanical scanning.

Staring mosaic focal planes combine detectors and associated signal processing to perform their mission functions. The ideal staring mosaic focal plane assembly (FPA) comprises both infrared detection elements and all necessary signal processing electronics in a single compact package which receives electromagnetic radiation and converts that into usable data. It is desirable to minimize: the number of electrical interconnections, power consumption and system weight, and to reject unwanted spurious signals and background clutter. However, the state-of-the-art in the necessary fabrication technologies does not yet allow this goal to be achieved. As a result, some portion of the signal processing is remotely located from the FPA in all concepts of staring mosaic FPA work presently in development. The relative distribution is dependent upon the basic architecture of the FPA.

Much of the current development work in staring mosaic focal planes is based on a planar architecture which attempts to approach a two-dimensional limit in order to achieve cost and weight reductions and shortened lead length between detectors and on-focal plane signal processing electronics. These concepts encompass both "monolithic" (detectors integral with focal plane signal processing electronics) and "hybrid" (detector arrays attached through bump bond contact to focal plane signal processing electronics) design approaches. An inherent constraint of planar concepts is that the detector area determines the space and topographical layout available for on-focal plane signal processing.

A natural alternative approach to these design configurations is not to compress the on-focal plane signal processing electronics to a planar (X-Y) configuration, but rather to use the space available in the Z-direction. This option employs a greater degree of on-focal plane signal processing by taking advantage of the larger packaging space, permitting the earliest possible discarding of unwanted information, thereby relieving the off-plane signal processing requirements.

A comparison of the Z-technology concept with the monolithic and planar hybrid approaches is illustrated Figure 1. The figure depicts the total signal processing divided into on-focal plane and off-focal plane portions. To a first approximation the sum remains constant for similar capabilities, and more on-focal plane processing requires less off-focal plane processing. Therefore, in comparing one approach to another, the merits of relative distribution between on- and off-focal plane should be examined from system considerations such as quality of clutter rejection, system weight and power consumption, etc.

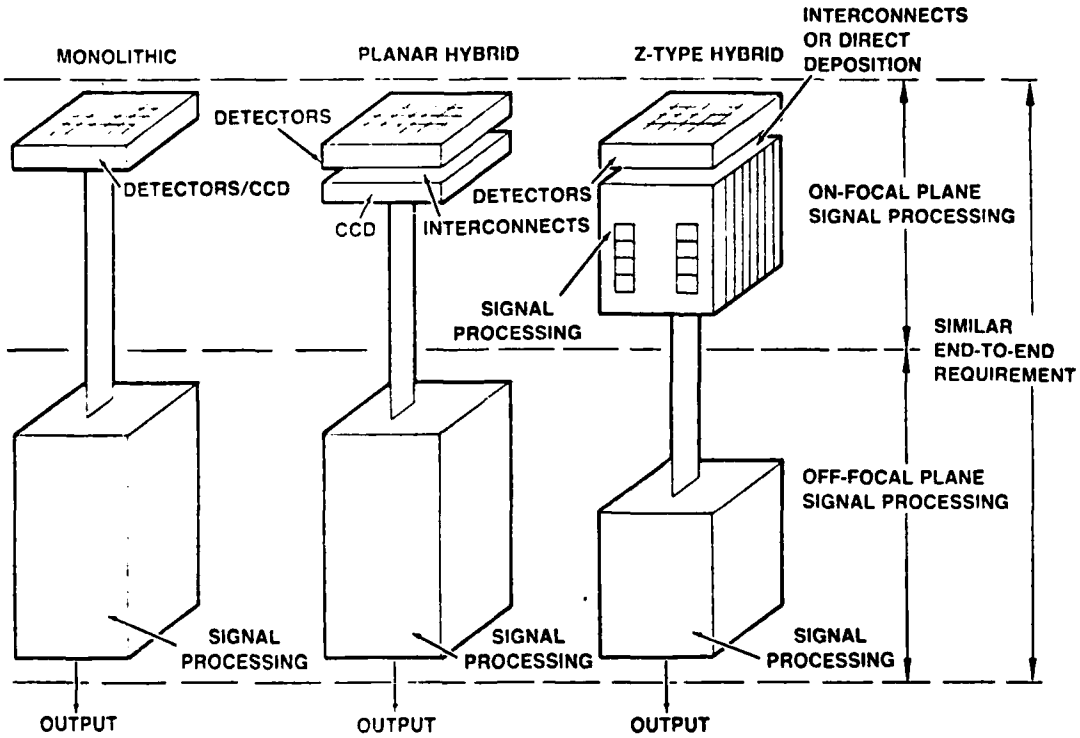

Figure 1. Mosaic Focal Plane/Signal Processing Configurations

Table I lists some of the features of the Z-technology. In contrast to the planar approaches for which the available on-focal plane signal processing area is approximately equal to the detector area, the Z-technology provides a signal processing area which is about 100 times the detector area. How this area is used to provide clutter rejection, dynamic range, and gain is explained in the table. In addition, mechanical and thermal issues such as fill factor, design flexibility and relative cooling requirements are discussed along with test and cost considerations.

TABLE I

FEATURES OF THE Z-TECHNOLOGY

1. Technical Performance

Clutter rejection	On-focal clutter rejection is possible through electrical passband filtering - switched capacitor filters are used with command control of low and high poles. Large area available for capacitors allows rejection of low frequency clutter, and large capacitance AC coupling to eliminate the DC background.
Dynamic range	Area available is used for large capacitances allowing large dynamic range. A large filter pole capacitance gives a low kT/C noise at one end, and a large fill/spill scupper capacitance gives large charge integration and gain which makes the downstream noise relatively small.
Fill factor	Considerably less dead space around modules since Z-technology uses imbedded leads rather than wraparound interconnects.
Survivability	Deeply buried signal processing provides insulation.
Gain	The large capacitance area allows net voltage gains to be achieved, providing high output voltage. The GAM-4 chip has a gain of 10.
Cooling requirement	The increased area of signal processing available typically does not require a much greater steady state cooling requirement than the corresponding planar architecture since most of the area increase is in capacitors rather than power consumption devices.

2. Fabrication

Design flexibility	The Z-configuration provides the designer with another degree of freedom, i.e., the amount of on-focal plane signal processing. The ratio of electronics area to detector area can be varied according to the particular requirements. Redundance circuitry may be provided to improve reliability or reduce failure modes.
Detector size	The Z-design by its nature accommodates reduced detector sizes without a corresponding reduction in signal processing volume or in size of signal processing chips. Only detector lead compression is required.
Detector subarray size	The current Z-design would allow single slabs of PV detectors up to 512 x 512 if they were available. Larger still signal processing sizes could be constructed without technology changes.
Weight	The Z-technology architecture incurs more weight on the focal plane. From a system point of view, this will be offset by the weight advantages achieved by the efficiency of early removal of unwanted information and reduction of off focal plane processing devices.
Test	The increased signal processing volume provides adequate room for test pads at intermediate points for each signal processing channel.

2. Fabrication (cont'd)

Cost	Repairability at low levels and intermediate test points allows efficient conservation of material. The Z-stack can be used as a common signal processing module which provides a base for different detectors and their unique optimized chips. The need for developing different interconnect schemes is avoided, leading to cost effectiveness. So far, design concepts have been developed for PbS, HgCdTe, and InSb using the common Z-technology.

Fabrication advantages of the Z-packaging technology are also discussed in the table. The underlying signal processing block uses a technology which today allows a 512 detector dimension. There is no developmental issue preventing a 512 x 512 dimension and, as two dimensional PV detector arrays grow from today's 32 x 32 and 64 x 64 sizes, they may be accommodated on this base without further development of the underlying electronics packaging. In fact, the Z-technology offers potential for development of a common signal processing module, i.e., a common interconnect scheme which can accommodate different detectors and their associated signal processing chips on a plug-in basis. This may prove to be cost effective since different interconnect developments would not be required for the different detector/signal processing sets.

Another feature of Z-packaging is the ability to handle increasingly smaller detector sizes (providing increased resolution or smaller optics sizes) without shrinking the electronics. With just lead density compression, the same signal processing chips may be used with very small detectors. Today's photolithographic and delineation technology will allow two mil detectors on two mil centers without additional risk.

When all of these tradeoff elements are evaluated, it is clear that the Z-technology has certain advantages, and should be pursued as an alternative architecture to the planar concepts for appropriate missions. After suitable design and research and development, the most cost effective approach for a given application will emerge.

For the Z-technology, the maximum cost effectiveness is expected to occur when the detectors are mounted directly on signal processing chips which extend into the Z-direction, thus eliminating the ceramic interface between the chips and the detectors. This will reduce cost and weight and result in a simpler system which still retains the advantages of the Z-technology.

Because of the Z-technology, advanced signal processing applications of mosaic focal planes can now exist. By making use of the volume available in the Z-direction, the proper microelectronics could be accommodated to handle the requirements of signal processing. The associated signal processing architecture, and its micro-electronic concepts are described in section 3.0.

The mosaic architecture involves the same bump bonding mating scheme used in planar hybrid focal planes yet some interface issues unique to Z-technology exist. These issues in addition to presenting alternative concepts for the electrical interface are addressed in section 4.0.

2.0 Research Objective

Conceive a design of the interface between a state-of-the-art photovoltaic array (32 x 32 or 64 x 64) and a Z-technology signal processing base. The design will address mechanical, electrical, and thermal features, and shall include conceptual design of signal processing chips.

3.0 Signal Processing Concept

3.1 Introduction

Because of the Z-technology advanced signal processing applications of mosaic focal planes can now exist. One of these applications, its associated signal processing architecture, and its microelectronic concepts are described here.

By making use of the volume available in the Z-direction, the proper microelectronics could be accommodated to handle the requirements for signal processing. Detection from a space-based focal plane is required of these signals exceeding a settable threshold. The repetition rate of the signals is 10 hertz and not more than eight lasers are expected to be emitting simultaneously, although 1024 focal plane pixels are needed to cover the area of possible laser sources. Classifying a detection is to identify its coordinates (pixel identification), its time of occurence, and its time duration which can range from 1 microsecond to 100 milliseconds.

Our approach to addressing these requirements is to place most of the signal processing functions before the multiplexing. Shown in Figure 2 is a simplified flow of the signal processing. Note that the signal processing flows on a per detector channel by channel basis. Because our application requires measuring a pulse duration which can range from 1 microsecond to 100 millisecond the functional cycle time of the signal processing structure must be as fast as 1 microsecond.

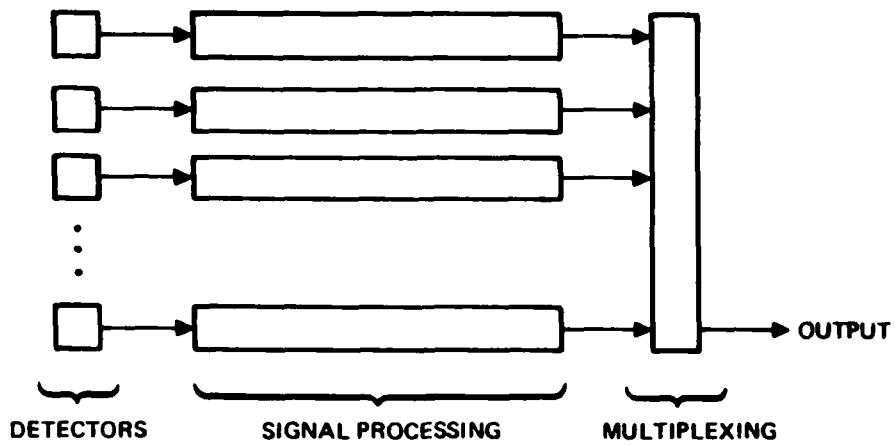

Figure 2. Z-Technology Approach

A hybrid/planar focal plane approach would place the multiplexing before most of the signal processing, essentially because there just isn't enough physical space to permit much processing per detector before the multiplexing. This hybrid approach is shown in Figure 3. Because our application requires measuring a pulse duration as short as 1 microsecond the functional cycle time of the signal processing structure must be fast enough to process the entire focal plane in 1 microsecond. With 1024 detectors, the signal processing and multiplexing frequency must be as fast as 1.024 gigahertz! This, of course, is not likely.

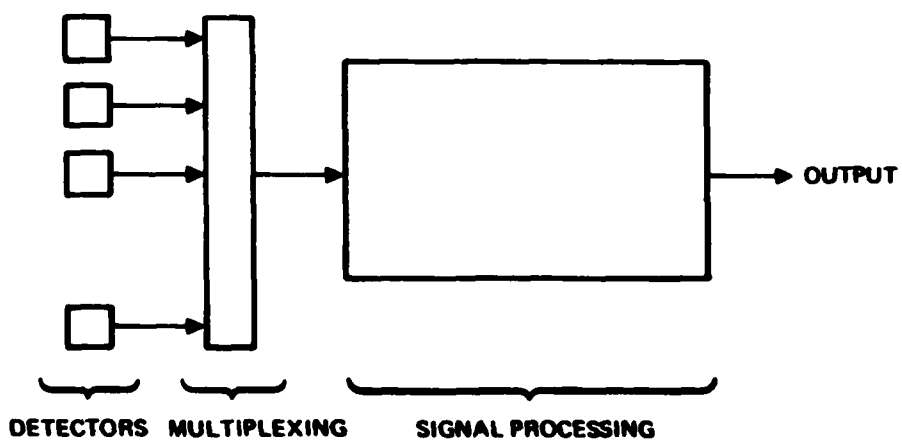

Figure 3. Hybrid/Planar Approach

Even by sectioning the focal plane for parallel processing, the processing frequency will still be intolerably high unless there is a very large number of sections. And as the number of sections is made large enough, the off-focal plane heat leaks will become intolerable. In short, the hybrid/planar approach is not practical for this application.

3.2 A Peak Detection/Signal Processing Multiplexer

The requirements discussed above call for a peak detection/signal processing multiplexer system. The heart of our proposed system is a microelectronic circuit which will provide most of the signal processing before the multiplexing. Shown in Figure 4 is a block diagram of the microcircuit's functions.

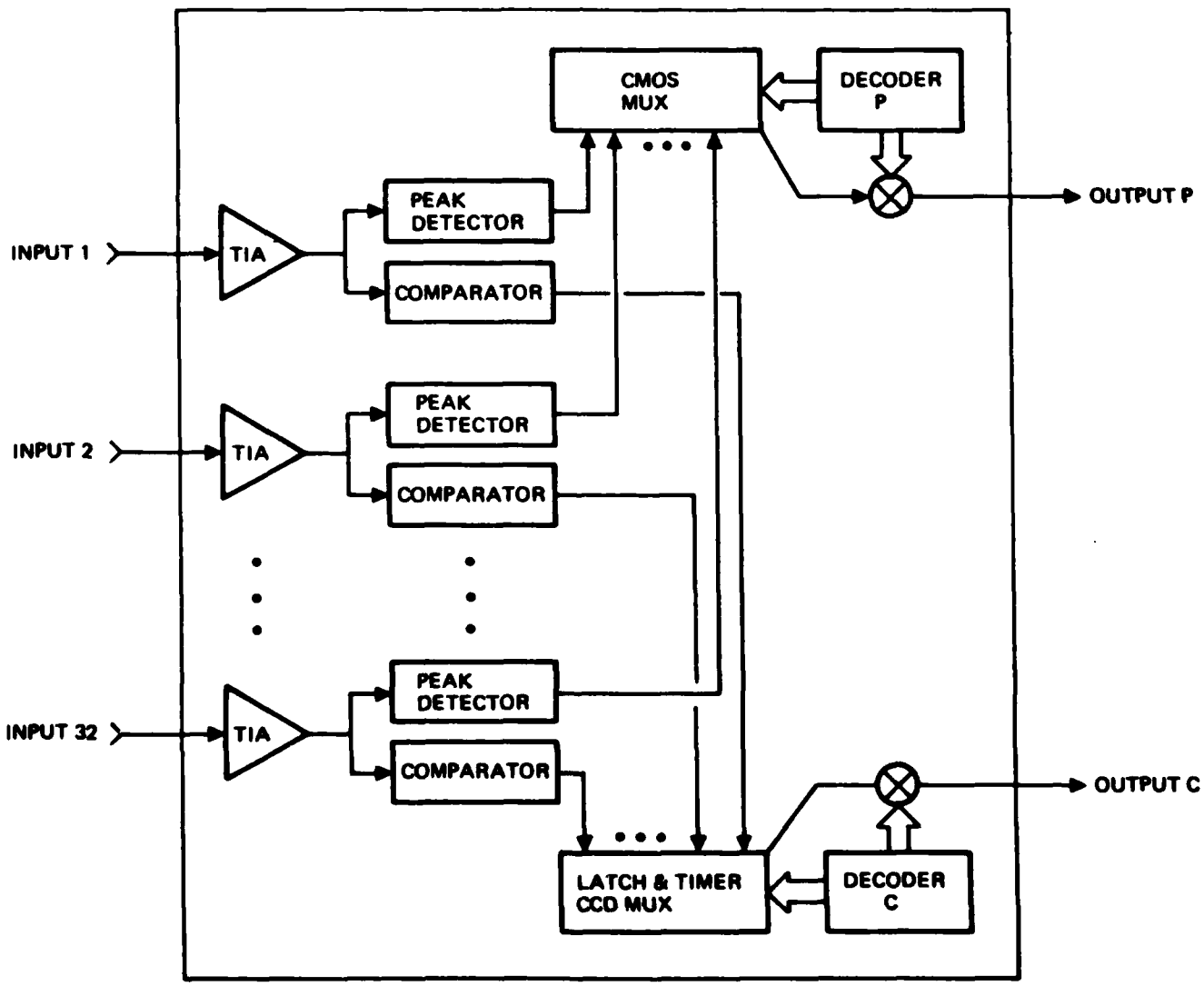

Figure 4. Peak Detection/Signal Processing Multiplexer

The microcircuit has inputs for 32 photovoltaic detectors. Each input channel has its own transimpedance preamplifier for interfacing with the detectors. Each preamplifier feeds both a voltage peak detector and a voltage comparator. The data from the comparators are multiplexed out serially from a charge-coupled device which has for its 32 parallel inputs, latches and timers. The peak detector data are randomly multiplexed out by the CMOS multiplexer. And control of the multiplexing is governed off-module by a microprocessor through the decode P and C switches.

Thirty-two of these chips are required to service the 1024 detectors in the focal plane. The number of output lines servicing the focal plane is two. Shown in Figure 5 is this general multiplexing scheme.

A description of the different functions of the chip will be discussed below.

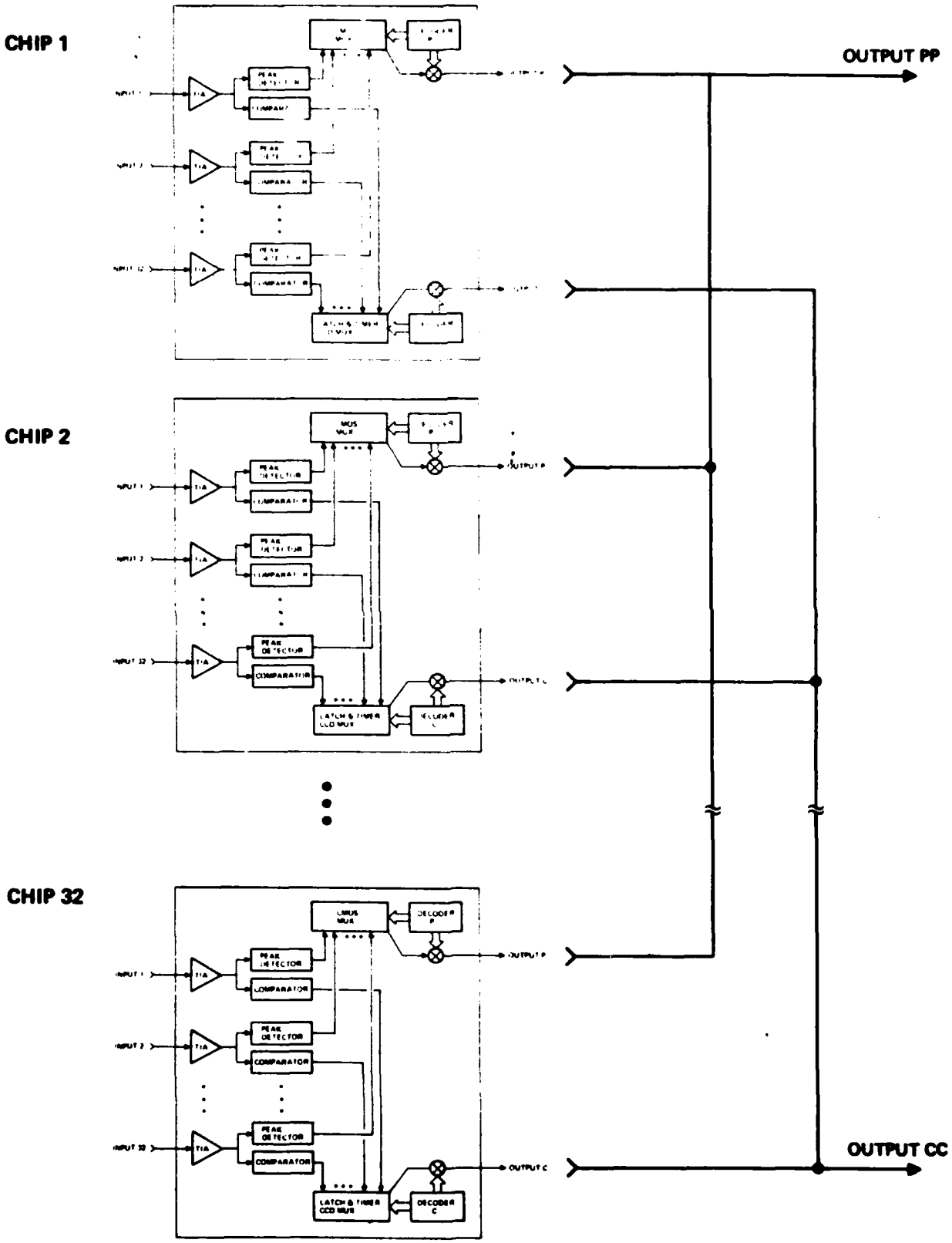

Figure 5. General Multiplexing Scheme

3.3 Decoders

The decoders receive their inputs from the microprocessor controller for the proper chip and channel select in implementing the general multiplexing scheme (Figure 5). Decoder P controls the chip and channel selection of Output P. Decoder C controls the chip selection of Output C.

Decoder C has a pair of positive and negative (or true and false) logic inputs for each of its six address lines. By wire bonding to either the positive or negative input for each address line, 32 different addresses --(one for each chip)-- are gotten. Decoder P is similarly constructed.

3.4 Transimpedance Input Amplifier

A schematic of the input amplifier is shown in Figure 6 along with the supporting bias circuitry. The amplifier is composed of two FETs. FET Q2 is operated below saturation and provides an impedance match to the detector. The other FET, Q1, is operated in the subthreshold region of conduction and acts as a relatively low impedance path to the load, R_L. The voltage across R_L is fed into a source follower buffer amplifier so that there is no loading on the pre-amplifier.

The common bias circuit sets the quiescent operating point of the FETs in the preamplifiers, of which there is one for each of the 32 detector channels.

The reverse bias provided is 100 millivolts. The minimum dynamic resistance expected from the photovoltaic detectors is 2.5×10^8 ohms. At that impedance the injection efficiency shall be greater than 85 percent. The preamplifier noise shall match that of the detector and the transimpedance gain shall carry the detector/preamplifier noise level above the remainder of microcircuit.

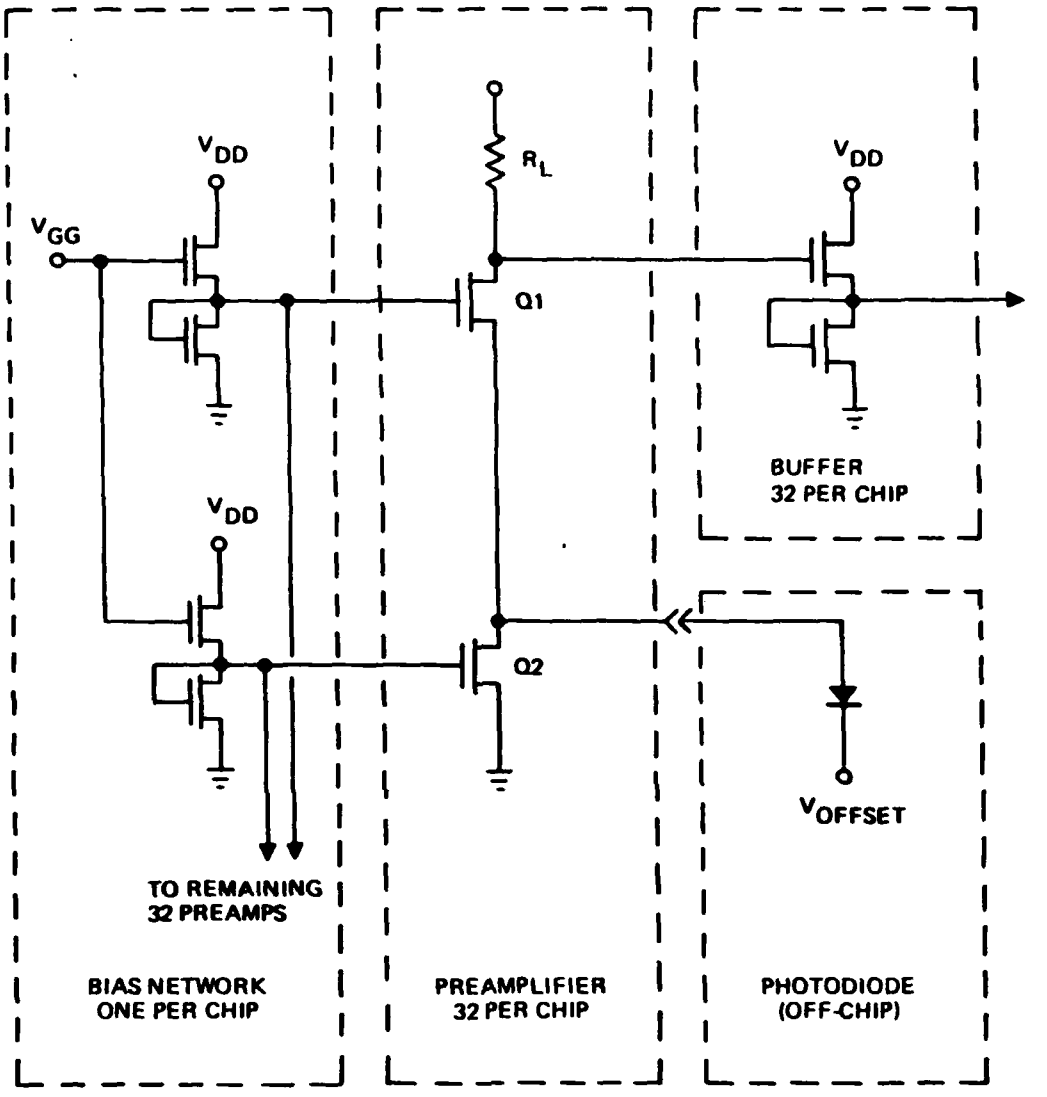

Figure 6. Transimpedance Amplifier

3.5 Peak Detectors

The peak detector is a modified fill-and-spill structure. Figure 7 shows the potential profile operation of the structure.

Initialization of the structure requires emptying the signal well and filling the reservoir with charge. This is accomplished by first clocking the signal well high and the reservoir low while fill-and-spilling into the reservoir with the input diode over the Tx gate. Then the signal well is clocked low and the channel access gate is clocked high.

A peak signal, shown going negative in Figure 7, on the signal gate can now be detected in the amount of charge allowed to equilibrate over the reservoir into the signal well. This captured charge is read by lowering the channel access gate so that the charge dumps onto a floating gate output structure. Each of the 32 peak detector outputs is addressed separately by turning on one of the L1 through L32 gates. Reset FETs exist to clear all the outputs.

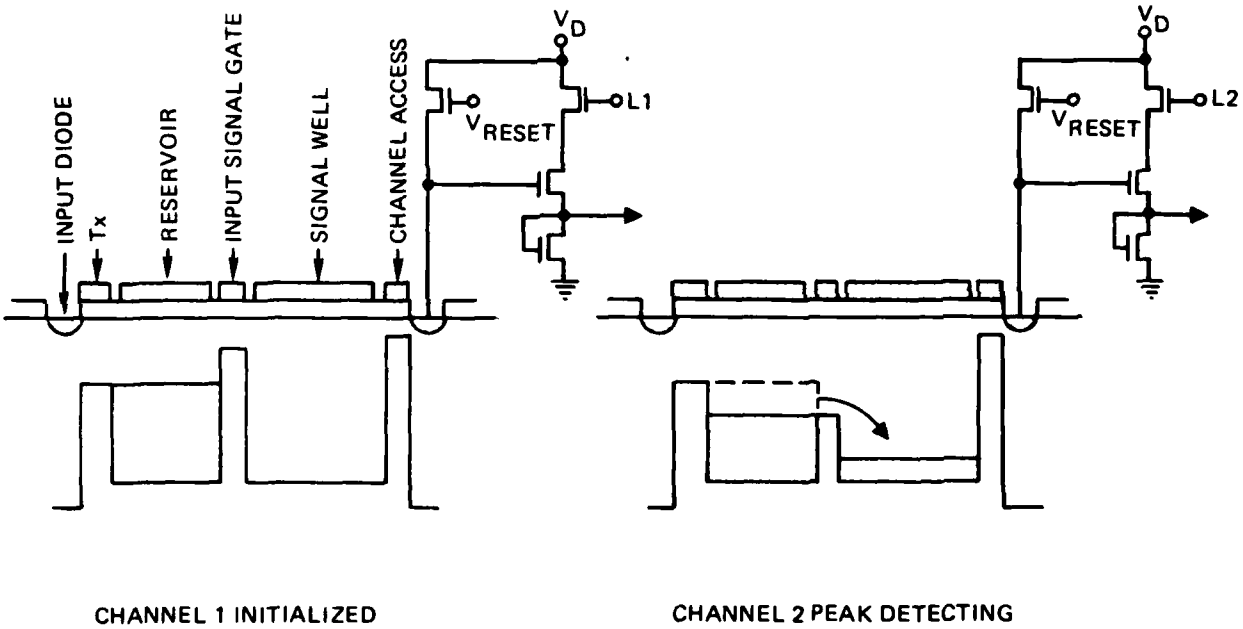

Figure 7. Peak Detector

3.6 Comparator

The comparator is a CMOS operational amplifier as shown in Figure 8. The threshold level is applied through one branch of the differential stage while the input is applied through the other. When the input exceeds the threshold the output is activated. There is no resetting or memory in the comparator: when the input ceases to exceed the threshold the output returns to its off state. Recording a threshold exceedance is achieved in the stage fed by the comparator, the latch and timer CCD multiplexer.

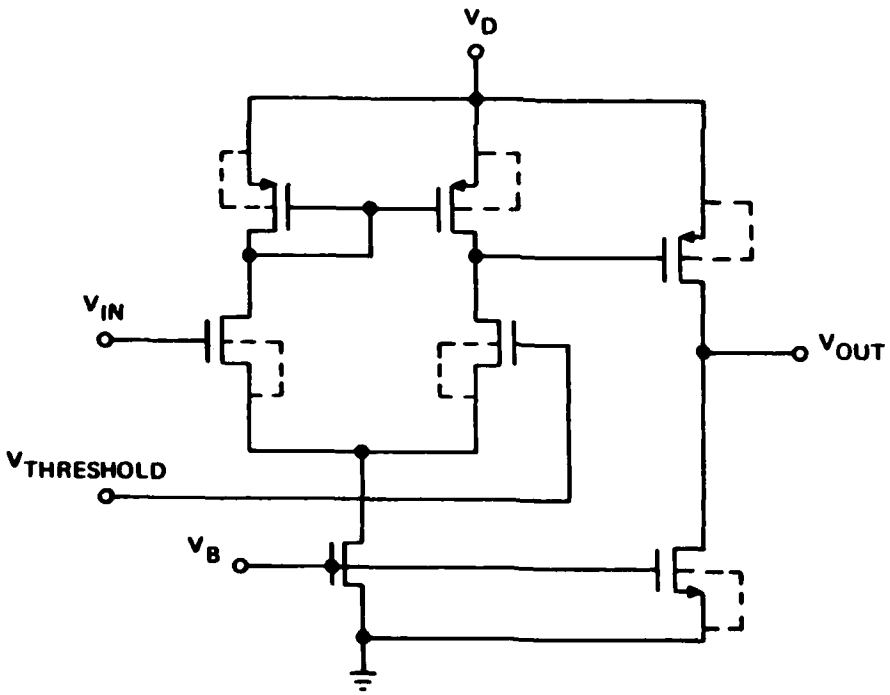

Figure 8. CMOS Comparator

3.7 Latch and Timer CCD Multiplexer

Because the comparator's output returns to the OFF state when its input ceases to be above the threshold, a memory or latching circuit is needed to record this information. The latch and timer charge-coupled device multiplexer (LTCCD) fills this need. The LTCCD also records the time duration of the signal exceedance. This information from each of the 32 channels is loaded in parallel into a charge-coupled device which then serially multiplexes it off chip (Output C).

Figure 9 is a voltage potential diagram of the latch and timer circuit. Figure 10 is its timing diagram. The circuit is similar to a multiple-fill-and-spill structure. The input diode is pulsed 256 times in a 256 microsecond period. If the comparator output is OFF during this period, charge is not trapped in the scupper and hence no charge is passed into the buffer storage. However, when the comparator output is ON, charge is trapped in the scupper and passed into the buffer storage. This fill-and-spill action will continue as long as the comparator output is ON. Thus the buffer storage will contain an amount of charge directly proportional to the time duration of the threshold exceedance in a 256 microsecond period. At the end of this period the charge in each of the 32 buffer storages are transferred into the CCD and are clocked out serially.

If the comparator output remains ON in the next 265 microsecond period, the timing of its duration will simply continue via the multiple fill-and-spills.

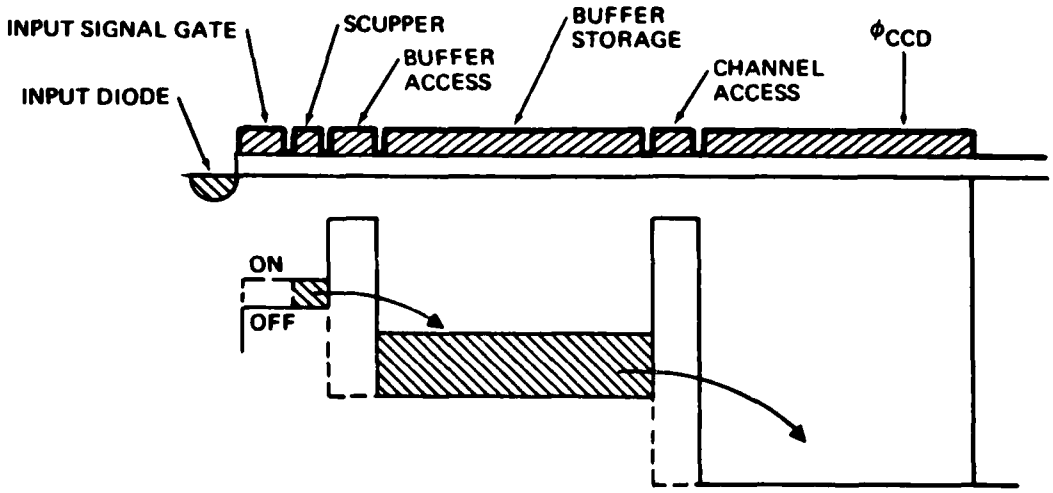

Figure 9. Latch and Timer Structure

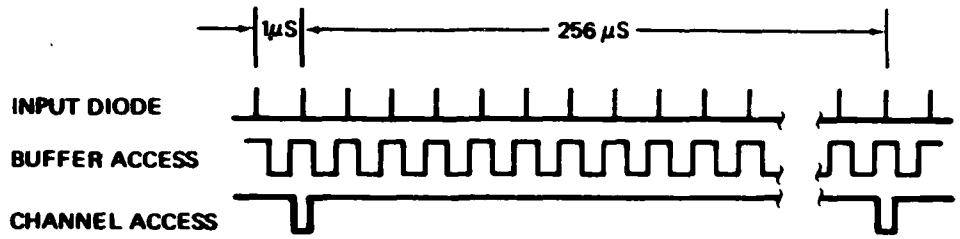

Figure 10. Latch and Timer Timing

3.8 Microprocessor Control

Figure 5 shows the general multiplexing scheme. The outputs CC and PP feed a microprocessor controller which governs the scanning of the data channels in search of threshold exceedances and the reading of the appropriate peak detector channels.

When this system is initialized, chip 1 is selected. After the first 256-microsecond frame time, the latch and timer CCD multiplexer of this chip is read. From the data the microprocessor is informed if there were any threshold exceedances during that frame time. If there were, the microprocessor takes note of their identify and the duration of the exceedances and the time of occurrence. Then chip 2 is selected and its latch and timer CCD is read, and so on until all 32 chips are read.

On the second and subsequent times around in reading the LTCCDs, the controller identifies new exceedances as well as recognizing the cessations of exceedances. A cessation alerts the controller to read the appropriate chip and channel for the peak value of that exceedance through output PP. Reading output PP for the different peak values is accomplished in real time against reading output CC.

A flow chart describing the microprocessor controller's function is shown in Figure 11. As can be seen, the provision provided to handle an overload of exceedances is to simply continue processing the exceedances which the controller can handle while ignoring the others.

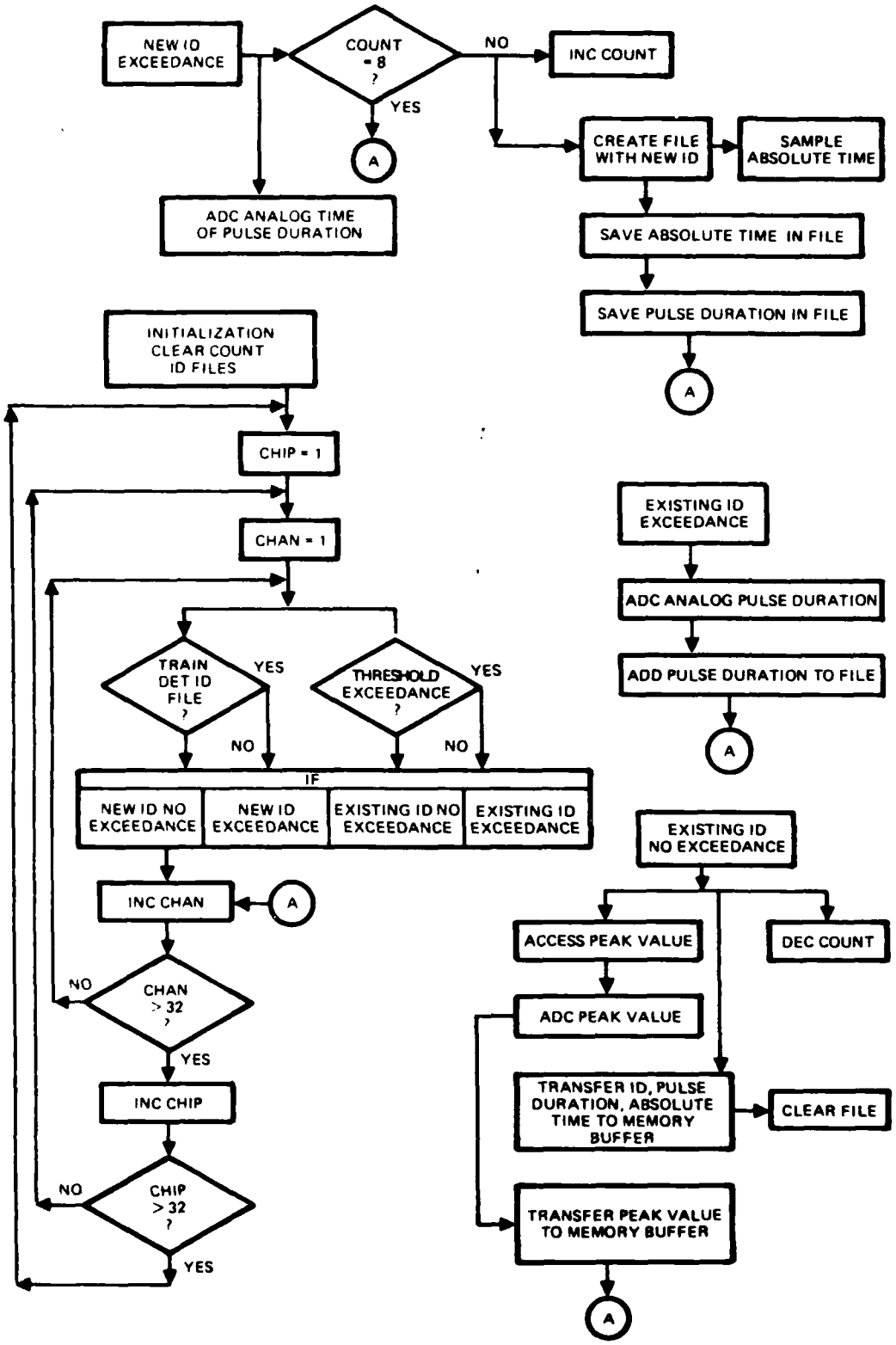

Figure 11. Microprocessor Controller Function Flow Chart

4.0 Detector Array Attachment Concept

4.1 Design Considerations

Figure 12 illustrates the structure of a typical Z-technology focal plane module. The module is a laminated structure composed of eight (in this case) alumina ceramic substrates upon which are printed leads. The leads serve to conduct the detector signals to signal processing chips which are bonded into wells formed by the laminated assembly. B-stage epoxy bonding sheets placed between the ceramic substrates are cured under pressure and temperature to form the structure. When the epoxy sheets are inserted, the ceramic surfaces at the detector end of the laminate are purposely kept free of epoxy so that a thermosetting material can be "wicked" in later. After these operations have been completed the end of the module is then "dressed" in preparation for the detector mating processes. The dressing operation exposes the ends of the printed detector interconnect leads. CrAu is then deposited on the module end surface thereby providing ohmic contact with each lead. These are electrically separated from each other by chemical etching to form bonding pads as shown in Figure 13. The detector interface thus comprises thin-film metallization on a ceramic-epoxy base structure.

The design of the detector-module interface must accommodate the aforementioned module structure while maintaining satisfactory electrical performance and compatible thermal, mechanical, and chemical characteristics. Preliminary analyses for a staring mosaic sensor using PV HgCdTe photodetectors have established the following minimum requirements for these characteristics:

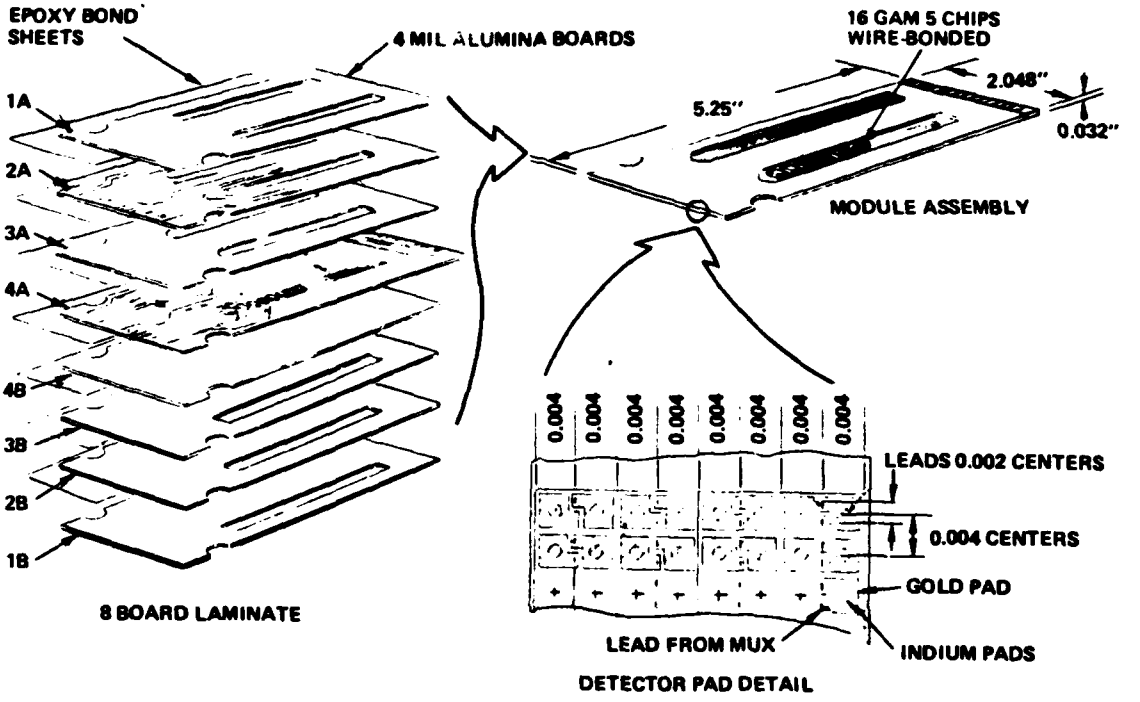

Figure 12. Z-Technology Focal Plane Module

CHARACTERISTICS

Electrical -

Contact resistance	<100Ω
Lead-Lead isolation	$<10^{12}\Omega$

Thermal -	
Conductivity	Dependent on required cool-down time and capacity
Mechanical -	
Tensile strength	$\leq 10^{-3}$g/detector element
Shear strength	$\leq 2(10)^{-3}$g/det.
Chemical -	
Compatibility	No mutual degradation

Besides providing good electrical contact, the attachment of the detector to the substrate must be of sufficient mechanical strength to preclude separation or dislocation because of heat, mechanical shock, vibration, and other environmental loads. The interface must also be thermally matched to minimize differential expansion stresses as well as to provide a good conductive heat path from the detectors to the cooling system interface.

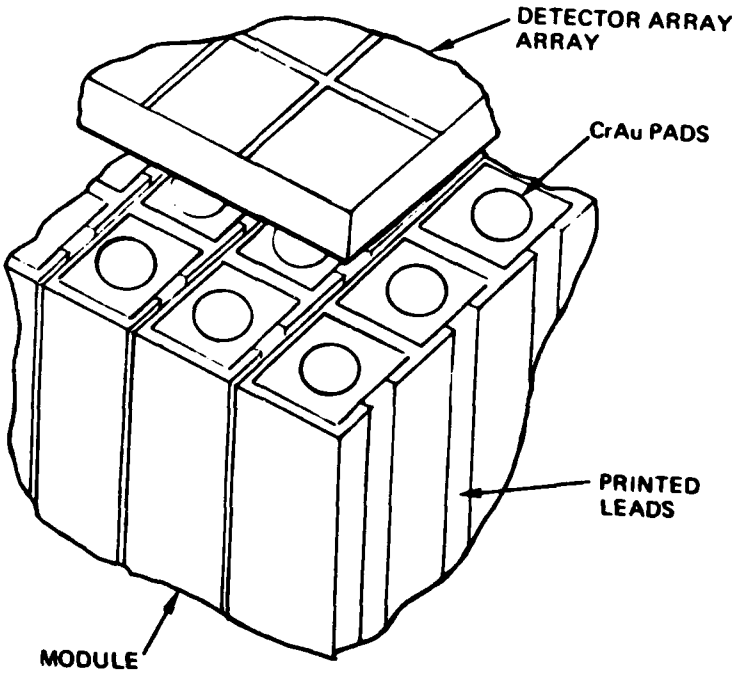

Figure 13. Relationship of Detector Array to Module Bonding Pads

4.2 Hybrid Attachment Schemes

There are two basic methods conceived for mating mosaic detector arrays to the module. In the first scheme, a flip-chip arrangement is used to electrically connect either a front- or backside- illuminated detector chip to the bonding pads on the module end. The interconnecting metal used should be a ductile metal such as PbSn or Indium joined by compression cold welding or reflow soldering. This method has been successfully applied to planar hybrid arrays containing 32x32 photodiodes on 100 μM centers and appears to be readily adaptable to Z-technology modules.

4.3 Flip-Chip Bump Bonding

Figures 14 and 15 illustrate the flip-chip "bump-bonding" scheme as applied to Z-technology modules. The mating indium bumps are formed in the following manner. Bump bonding a detector array to a single module, a group of modules, or any flat electronic substrate requires as a minimum, a single conductive bump on either the array or the electronic substrate and a conductive pad on the mating surface. However, it is more desirable to have a conductive bump on both surfaces to minimize the flatness requirements on the mating surfaces and the height-to-width ratio required for the individual bump. In addition, mating bumps facilitate controlling bump collapse during bonding, thus providing better contact quality. One negative aspect of providing bumps on the two mating surfaces is that both sets of bumps must have tighter locational tolerances for alignment.

The metallic bumps must be formed in such a way that deformation will take place during the bond process. This will shatter any oxides which may have formed on the bump surface thus permitting a cold weld to form (see Figure 16). In some cases, ultrasonics have been used to assist in this process. Another method used to fracture the oxide is to so shape the bumps that they cause mutual deformation when mated. Alternately, one may use different materials or combination of materials

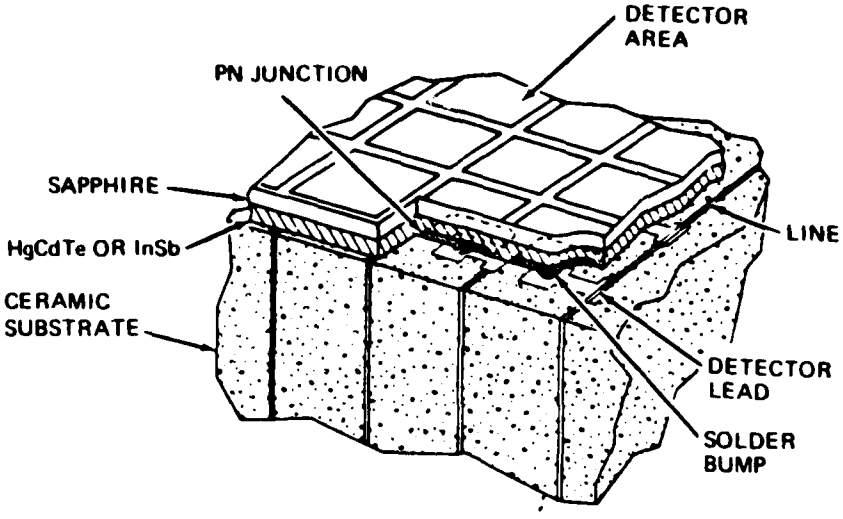

Figure 14. Cutaway of Bump Bonded Array

BUMP CONFIGURATION

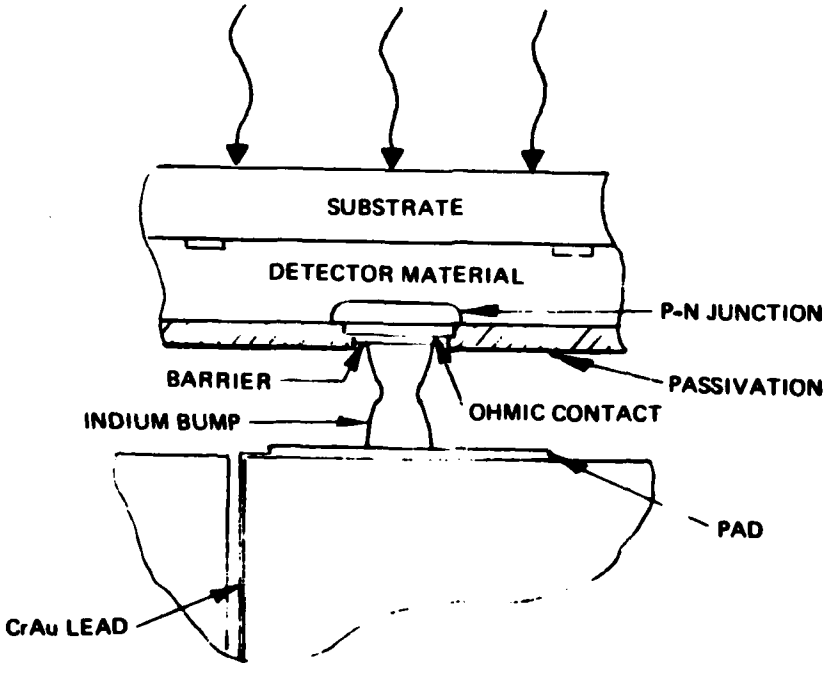

Figure 15. Exploded View of Bump Bonded Array

or combination of materials in opposing bumps. In this way the more rigid bump may cause the second bump to deform around it, causing the oxide layer to shatter, thus forming a cold weld (see Figure 17).

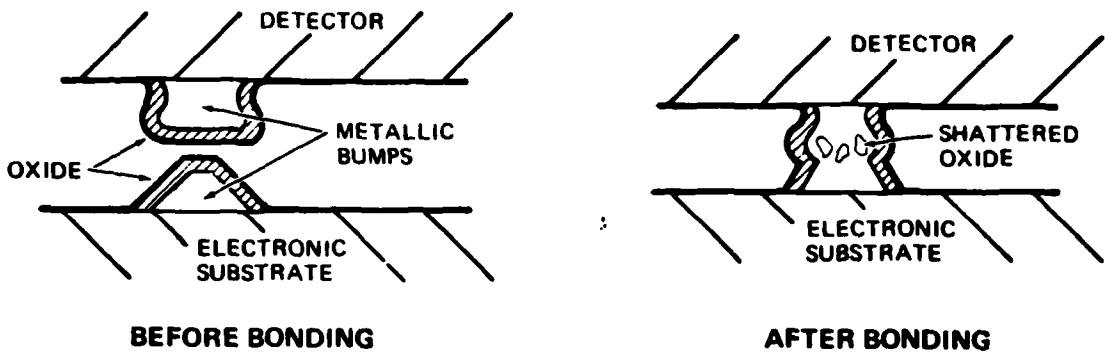

Figure 16. Cold Weld Bump Bonding (Like Materials)

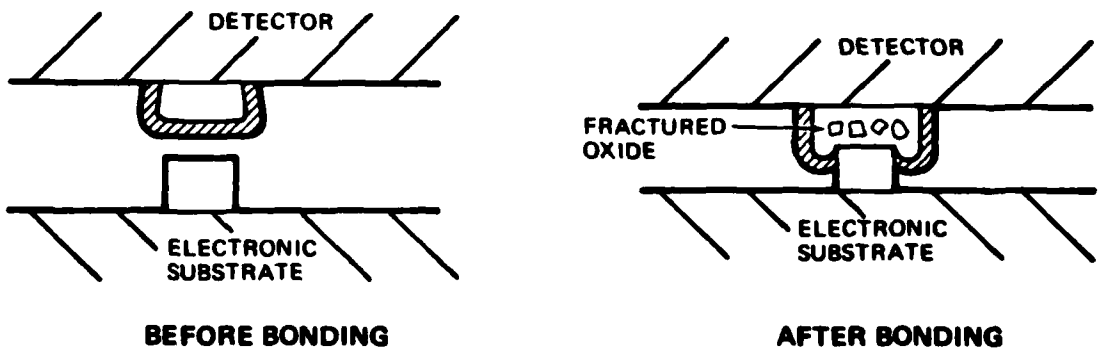

Figure 17. Cold Weld Bump Bonding (Different Materials)

4.4 Adhesive Bonding

A second method of attaching detector arrays to Z-technology modules is presently under development by New England Research Corporation (NERC). This technique is illustrated in Figure 18. While the detail process of attachment is held to be proprietary by NERC, the general approach is as follows.

A polished HgCdTe plank is first bonded to the metallized end of the module with a conductive epoxy adhesive. It is further lapped to the desired thickness and then ion-milled through the plank and the epoxy to form individual mesas or islands. The gap thus formed is then filled with a non-conductive epoxy which gives some structural support as well as optical isolation between photodiodes. The HgCdTe then is exposed to several proprietary processes which serve to activate the material. These processes are completed with the deposition of a common electrode over the epoxy spacer material.

The potential advantages of this detector attachment method are improved specific detectivity, elimination of optical crosstalk within the detector substrate, improved edge-detector yield, and excellent heat transfer characteristics. One disadvantage is the higher potential for damage to the mating submodule through the myriad processing steps.

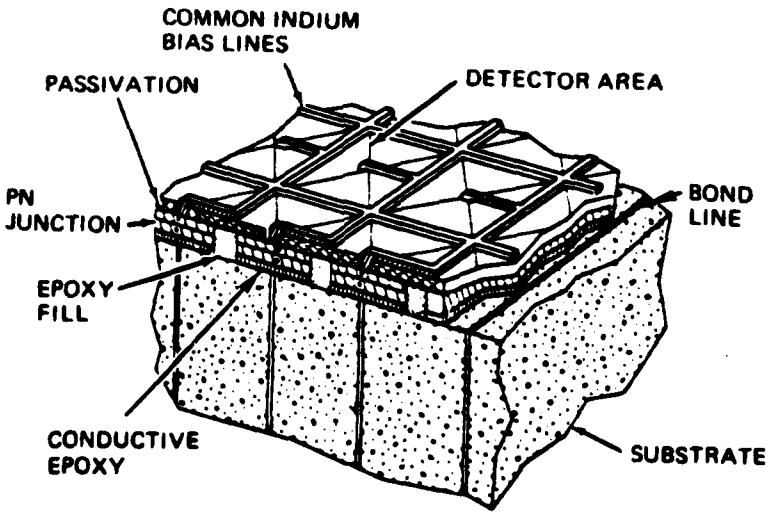

Figure 18. Cutaway of NERC Approach to Array/Module Interface

4.5 Experimental Bump Formation

For limited numbers of hybrid arrays, one may hand place performed indium balls on one or both of the mating surfaces before joining the array using a combination of pressure and heat. Although this method would be very time consuming and inefficient, its advantages are that almost no specialized equipment is required and the system can be set up quickly for small runs. Once again the planarity of the mating surfaces must be accurately maintained.

One way to facilitate ball placement is to use a perforated mask placed in contact with the surface which is to have bumps attached to it. Then, while the mask and substrate surface are gently vibrated, presized indium balls are poured over them. After the mask perforations have been filled with indium balls, the excess are poured off. A Teflon-coated roller is then used to cold weld the balls to the mating metal pads below (see Figure 19). After the mask is removed, the mating surfaces are aligned and bonded. An alternative to the Teflon roller is to heat the substrate holding the indium balls to join the indium to the metallized pads before the mask is removed.

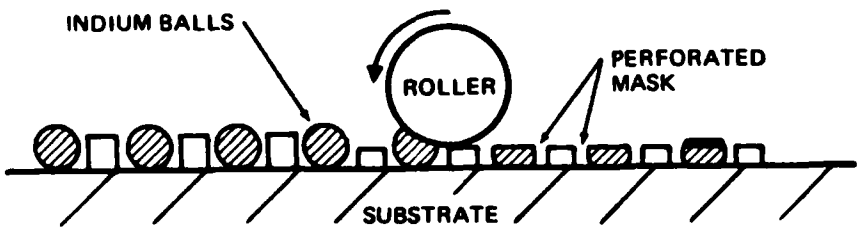

Figure 19. Alternate Approach for Small Quantity

4.6 Solder Reflow Method

Another method of forming indium bumps on a substrate would be to first passivate the areas of the surface which are not to have indium bumps joined to it. Then use solder flow techniques to form the pedestals on the unpassivated areas. A problem with this scheme is that it would cause large heat loads to be placed on the substrate from the solder bath. This heat load might be reduced by depositing a heavy coat of indium over the entire surface, then using heated gas to cause the indium to flow, allowing surface tension to pull it into pedestals in the unpassivated areas.

4.7 Chemical Deposition

The aforementioned methods of bump formation have a major drawback in that the ability to shape the pedestals is limited. One method of forming shaped pedestals is to use a system of successive masks and chemical deposition. Obviously, this method is limited to substrates which can be treated without being damaged by chemical treatment. One way around this problem is to grow shaped pedestals on a glass or Kapton substrate by means of successive chemical depositions. Once the desired shape has been grown, the pedestals are transferred to the substrate by means of a light pressing or rolling operation. It has been found that a mushroom shaped pedestal works well in bump bonding operations. This shape is difficult to produce on a substrate, but can be easily produced in an inverted shape on a carrier and transferred to the substrate. The ability to transfer the indium pedestals with very light pressure is possible because of its ability to form cold welds easily.

One way to produce indium pedestals in large quantities for later transfer onto a substrate would be to use a tool to stamp out an array of pedestals onto a non-adhering backplane. This stamped array would then be transferred onto the substrate. The fine indium connections left between the pedestals by the stamping process would then be separated by scribing.

As stated before, one of the main drawbacks of using indium bumps is that it is difficult to control the penetration of one bump into the other. A method of obtaining more control over penetration is to form one of the bumps from a harder material. Several methods of forming these strong bumps have been used. Some of these were the silver-gold and palladium nickel-gold bumps of the General Electric Mini Mod technique and titanium-palladium-gold bumps of the Honeywell Tab process.

A very simple method of obtaining a rigid pedestal, which can be placed very accurately on a delineated metallized substrate is to stitch wire the substrate with a thermal compression wire bonder. After the wire bonding process the wire would be pulled close to the T.C. bead, leaving an aluminum ball with a very short tail which could be used as one bump in a bump bonding process. It would also be possible to place T.C. bonds at only various predefined intervals and use these as spaces in an indium-to-indium bump bonding process.

4.8 Conclusions

No absolute conclusions can be drawn from the analyses of the aforementioned bump bonding techniques without actual hardware testing. It is recommended that a follow-on program address this much needed area of process development.

5.0 Risk Areas

5.1 Signal Processing

- Adverse effect of circuit complexity on yield
- High power requirements increase thermal loading
- Threshold uniformity of comparators
- Uniform signal resolution of the peak detectors
- Timing resolution of the Latch and Timer CCD, i.e., gate structure

5.2 Detector Array Attachment

- Lack of planarity which may consume focusing tolerances of intended system
- Bump bonded arrays may fail due to shorting of interconnects
- Delamination of detector array from the electronics may degrade or catastrophically terminate operation of system
- Adhesive bonds due to epoxies having high coefficients of thermal expansion compared to substrate materials may cause delamination
- During bonding process detector material may suffer damage

6.0 Summary

6.1 In the previous text we have recounted the research activities performed in accordance with the contractual Statement of Work. This research, we believe, has contributed significantly to the advancement of the application of Z-technology to future surveillance systems. The next phase of activity should address producibility.

6.2 The risk areas associated with signal processing as detailed in paragraphs 5.1 should be addressed in a development program wherein hardware is produced and tested to "demonstration system" requirements. Performance parameters for the CCD's could be derived from existing programs such as Mini-HALO, Teal Ruby and MSP.

6.3 The next phase of activity in the area of bump bonding detector arrays to Z-technology modules needs be process development wherein the various attachment techniques addressed in paragraph 4.0 are examined in the context of the risk areas discussed in paragraph 5.2.

6.4 We recognize that these producibility efforts are not pure research and as such may not be in your interest to directly pursue. However, should the development of manufacturing processes of this nature interest you, we will be most willing to serve you.

DATE
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